Amendment to the Claims

The listing of claims below will replace all prior versions and listings of claims in the application.

1-3. (Previously Canceled)

4. (Previously Presented) A cross link multiplexer bus, comprising:

a plurality of cross link multiplexers, said plurality of cross link multiplexers having a destination port configured to receive a signal and an origin port configured to produce said signal; and

a plurality of interconnects, wherein a set of interconnects of said plurality of interconnects is coupled between a pair of adjacent cross link multiplexers of said plurality of cross link multiplexers;

wherein:

said signal is configured to be represented as a series of characters, and a character of said series of characters is configured to be represented as a first data bit, a second data bit, and a first control bit;

a first interconnect of said set of interconnects is configured to convey said first data bit, a second interconnect of said set of interconnects is configured to convey said second data bit, and a third interconnect of said set of interconnects is configured to convey said first control bit;

said first interconnect, said second interconnect, and said third interconnect are configured in a manner to reduce cross-talk;

said third interconnect is positioned substantially between said first interconnect and said second interconnect;

said series of characters is further configured to be represented as a third data bit, a fourth data bit, and a second control bit;

a fourth interconnect of said set of interconnects is configured to convey said third data bit, a fifth interconnect of said set of interconnects is configured to convey said

fourth data bit, and a sixth interconnect of said set of interconnects is configured to convey said second control bit; and

said sixth interconnect is positioned substantially between said fourth interconnect and said fifth interconnect.

5. (Original) The cross link multiplexer bus of claim 4, wherein said first interconnect, said second interconnect, said third interconnect, said fourth interconnect, said fifth interconnect, and said sixth interconnect are fabricated on a common layer within an integrated circuit chip, said common layer substantially defined by a plane.

6. (Original) The cross link multiplexer bus of claim 4, wherein:

said first interconnect, said second interconnect, and said third interconnect are fabricated on a first layer within an integrated circuit chip, said first layer substantially defined by a first plane; and

said fourth interconnect, said fifth interconnect, and said sixth interconnect are fabricated on a second layer within said integrated circuit chip, said second layer substantially defined by a second plane, said second plane substantially parallel to said first plane.

7. (Original) The cross link multiplexer bus of claim 6, wherein:

said fourth interconnect is positioned substantially adjacent to said third interconnect along a direction substantially perpendicular to said first plane and said second plane; and

said sixth interconnect is positioned substantially adjacent to said second interconnect along said direction substantially perpendicular to said first plane and said second plane.

8-10. (Previously Canceled)

11. (Currently Amended) A cross link multiplexer bus, comprising:

a plurality of cross link multiplexers, said plurality of cross link multiplexers having a destination port configured to receive a signal, an origin port configured to produce said signal, a first power supply configured to provide a first voltage, and a second power supply

configured to provide a second voltage, said first voltage is different from said second voltage; and

a plurality of interconnects, wherein a set of interconnects of said plurality of interconnects is coupled between a pair of adjacent cross link multiplexers of said plurality of cross link multiplexers;

wherein:

said signal is configured to be represented as a series of characters, and a character of said series of characters is configured to be represented as a first data bit and a second data bit;

a first interconnect of said set of interconnects is configured to convey said first data bit, a second interconnect of said set of interconnects is configured to convey said second data bit, and a third interconnect of said set of interconnects is configured to convey one of said first voltage and said second voltage;

said first interconnect, said second interconnect, and said third interconnect are configured in a manner to reduce cross-talk;

said third interconnect is positioned substantially between said first interconnect and said second interconnect;

said character of said series of characters is further configured to be represented as a third data bit and a fourth data bit;

a fourth interconnect of said set of interconnects is configured to convey said third data bit, a fifth interconnect of said set of interconnects is configured to convey said fourth data bit, and a sixth interconnect of said set of interconnects is configured to convey one of said first voltage and said second voltage; and

said sixth interconnect is positioned substantially between said fourth interconnect and said fifth interconnect.

12. (Original) The cross link multiplexer bus of claim 11, wherein said first interconnect, said second interconnect, said third interconnect, said fourth interconnect, said fifth interconnect, and said sixth interconnect are fabricated on a common layer within an integrated circuit chip, said common layer substantially defined by a plane.

13. (Original) The cross link multiplexer bus of claim 11, wherein:

said first interconnect, said second interconnect, and said third interconnect are fabricated on a first layer within an integrated circuit chip, said first layer substantially defined by a first plane; and

said fourth interconnect, said fifth interconnect, and said sixth interconnect are fabricated on a second layer within said integrated circuit chip, said second layer substantially defined by a second plane, said second plane substantially parallel to said first plane.

14. (Original) The cross link multiplexer bus of claim 13, wherein:

said fourth interconnect is positioned substantially adjacent to said third interconnect along a direction substantially perpendicular to said first plane and said second plane; and

said sixth interconnect is positioned substantially adjacent to said second interconnect along said direction substantially perpendicular to said first plane and said second plane.

15-17. (Previously Canceled)

18. (Currently Amended) A cross link multiplexer bus, comprising:

a first cross link multiplexer;

a second cross link multiplexer;

a destination port coupled to one of the first cross link multiplexer and the second cross link multiplexer and configured to receive a signal, wherein the signal is configured to be represented as a series of characters, a character of said series of characters is configured to be represented as a first data bit, a second data bit, a first control bit, a third data bit, a fourth data bit, and a second control bit;

an origin port coupled to one of the first cross link multiplexer and the second cross link multiplexer and configured to produce the signal;

a first interconnect coupled between the first cross link multiplexer and the second cross link multiplexer and configured to convey the first data bit;

a second interconnect coupled between the first cross link multiplexer and the second cross link multiplexer and configured to convey the second data bit;

a third interconnect coupled between the first cross link multiplexer and the second cross link multiplexer, said third interconnect positioned between the first interconnect and the second interconnect in a manner to reduce cross talk, and configured to convey one of the first control bit, a power supply voltage, and a ground voltage;

a fourth interconnect coupled between the first cross link multiplexer and the second cross link multiplexer and configured to convey the third data bit;

a fifth interconnect coupled between the first cross link multiplexer and the second cross link multiplexer and configured to convey the fourth data bit; and

a sixth interconnect coupled between the first cross link multiplexer and the second cross link multiplexer, said sixth interconnect positioned between the fourth interconnect and the fifth interconnect in ~~a~~ the manner to reduce cross talk, and configured to convey one of a second control bit, the power supply voltage, and the ground voltage.